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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,325	04/28/2004	Kenneth L. DeVries	BUR920030184US1	3324

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EXAMINER	
IM, JUNGHWA M	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 01/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/709,325	DEVRIES ET AL.	
	Examiner	Art Unit	
	Junghwa M. Im	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10,19 and 20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,19 and 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 June 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/28/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election with traverse of claims 1-10 and 19-20 in the reply filed on November 3, 2005 is acknowledged. The traversal is on the ground(s) that the sequence of the interconnection matters rather than the type of a process used, and there is no added burden for the examiner to examine both of the product and the process claims since there are closely related. This cannot be found persuasive since Applicants' arguments are not clear. In order to have this restriction requirement reconsidered, Applicants are required to specifically states in the record that device and making device are not patentably distinct and explain how they are not patentably distinct, i.e., that the electronic chip must and will have a recognizable structure or feature due to plasma processing, not what is seen during the manufacturing process. Therefore, the restriction requirement is not held final at this time until Applicant responds.

Claim Objections

Claim 5 is objected to because of the following informalities. Claim 5 recites "between first grid" which should be -- between said first grid --. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1, 4-6 and 19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites a unclear limitation of "said first grid and said second grid are interconnected in a fabrication layer no later than a first metallization layer of said chip that accumulates a charge during a plasma process in said fabrication." This limitation is confusing since it is apparent in Figures of the instant invention that the first metallization layer is also the first and the second grid. Additionally, it is also confusing to understand how two grids are interconnected no later than a first metallization layer of said chip that accumulates a charge during a plasma process. Note that the first metallization layer starts accumulating a charge once it is formed by plasma processing. Therefore, it is confusing to understand how the first and the second grids are connected even before the first metallization layer (for both the first and the second grid) is formed. Furthermore, it is confusing if "said fabrication" is implied for an interconnection, plasma processing or a step of forming a fabrication layer.

Claim 19 recites a unclear limitation substantially identical in nature to the one in claim 1.

Claim 4 recites a limitation, "a diffusion region; ... a source of a field effect transistor... and a drain of said field effect transistor ..." Note that a diffusion region is a source and a drain region. Claim 4 further recites a limitation of "a first metallization layer" while claim 1 also recites 'a first metallization layer."

Claim 5 recites a limitation of "an interconnect ... is conductive." It is apparent that "an interconnect" is an action of interconnecting since there is no interconnect structure between the first

and second grid in the instant invention. Thus, it is unclear how the interconnecting action is conductive.

Claim 6 recites a unclear limitation of "wherein said chip comprises components fabricated in a layer that has substantially no leakage of carriers to a substrate of said chip." It is confusing since the instant invention does not disclose this aspect at all. At best the instant invention discloses that the invention is intended to provide a solution to breakdown problems during plasma processing when there is no leakage of the carriers to the substrate.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-6, 8-10 and 19 are rejected under 35 U.S.C. 102(e) as anticipated by Liu et al. (US 6869844), hereinafter Liu.

Regarding claim 1, insofar as understood, Figure 1 of Liu shows an electronic chip, comprising:

a first circuit design module having a first grid [14]; and

a second circuit design module having a second grid [12],

wherein said first grid and said second grid are interconnected in a fabrication layer.

Note that "no later that a first metallization layer of said chip" and "a plasma processing" are a process designation, and would thus not carry patentable weight in this claim drawn to a product. See *In re Thorp*, 227 USPQ 964 (Fed. Cir. 1985).

In addition, there is no charge accumulation in the device of Liu in Figure 1 during a plasma process in the fabrication since a protective circuit [20] is formed (col. 3, lines 26-37).

Regarding claim 2, Figure 1 of Liu shows at least one of said first grid and said second grid comprises a metallization grid (metal interconnect; col. 1, line 50).

Regarding claim 3, Figure 1 of Liu shows said first grid and said second grid comprise one of a power grid and a ground grid (Note that the interconnection lines form the circuits 12, 14 are connected to a source and a drain).

Regarding claim 4, insofar as understood, Figure 1 of Liu shows said first grid and said second grid are interconnected by at least one of: a diffusion region [source/drain]; a gate of a field effect transistor; a source of a field effect transistor connected to said first grid and a drain of said field effect transistor connected to said second grid; a local interconnect; and a first metallization layer that is designed to electrically interconnect at a boundary of said first circuit design module and said second circuit design module.

Regarding claim 5, insofar as understood, Figure 1 of Liu shows that first grid and said second grid are conductive during said plasma processing because of the charge accumulation and is nonconductive during an operation of said chip unless activated by a signal because of a protective circuit [20].

Regarding claim 6, insofar as understood, Figure 1 of Liu shows that said chip components/interconnect is fabricated in a layer that has substantially no leakage of carriers to a substrate of said chip because of the protective circuit.

Regarding claim 8, it is inherent/obvious that Figure 1 of Liu shows that said layer is temporarily activated by said plasma processing (because of the charge accumulation) such that carriers in said layer are migratable during said plasma processing (before the formation of the protective circuit).

Regarding claim 9, it is inherent/obvious that Figure 1 of Liu shows that at least one of said first grid and said second grid comprises a metal grid that includes a predetermined surface area of at least one of said first circuit design module and said second circuit design module.

Regarding claim 10, Figure 1 of Liu shows an electronic chip fabricated in accordance with claim 1 (memory chip in computer; col. 1, lines 12-13).

Regarding claim 19, insofar as understood, Figure 1 of Liu shows an electronic apparatus comprising:

at least one electronic chip [10], comprising:

a first circuit design module having a first grid [14];

a second circuit design module having a second grid [12]; and

means [20; protective circuit] for electrically interconnecting said first grid and said second grid no later than a first metallization layer that accumulates a charge during a plasma process in a fabrication of said chip.

Note that "no later that a first metallization layer of said chip" and "a plasma processing" are a process designation, and would thus not carry patentable weight in this claim drawn to a product. See *In re Thorp*, 227 USPQ 964 (Fed. Cir. 1985).

In addition, there is no charge accumulation in the device of Liu in Figure 1 during a plasma process in the fabrication since a protective circuit [20] is formed (col. 3, lines 26-37).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 7 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Liu in view of Kimura (US 6815771).

Regarding claim 7, Figure 1 of Liu shows most aspect of the instant invention except "said chip includes a silicon on insulator (SOI) structure." Fig. 12 of Kimura shows a chip includes a silicon on insulator (SOI) structure (col. 1, lines 12-15). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Kimura into the device of Liu in order to have said chip including a silicon on insulator (SOI) structure to alleviate the problem of breakdown voltage.

Subject matter regarding claim 20 has been discussed in claim 7.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junghwa M. Im whose telephone number is (571) 272-1655. The examiner can normally be reached on MON.-FRI. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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